VLSI Testing Homework 3

系所：資應所

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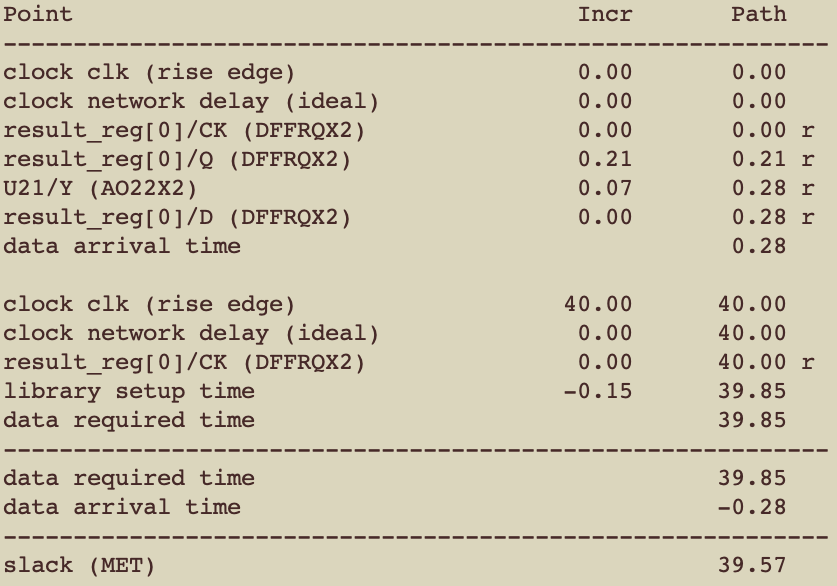
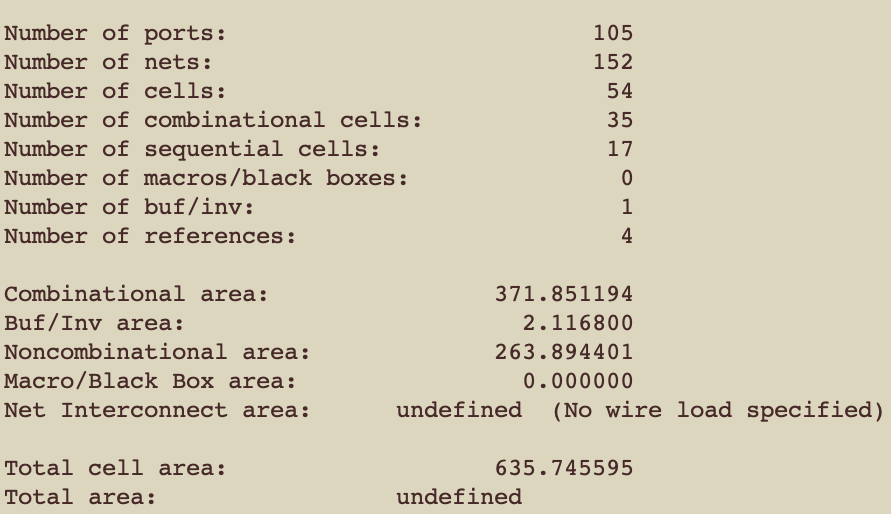
學號：109065520

1. Derive the logic circuit of a 16-bit adder

Input : 2 16-bits data

Output : 1 17-bits result

Synthesis result of my adder with period = 40ns by Design compiler :



1. My BISTed circuit
   1. top.v : Connect all modules.
   2. adder.v : Add two 16-bits data into 17-bits result.
   3. LFSR.v :

Characteristic polynomial: g(x) = x^7 + x^1 + 1

I use 6 LFSRs to generate two inputs of adder.v. Each LFSR has a unique random seed.

* 1. LFSR\_manager.v :

I use 2 LFSR\_managers to generate 2 16-bits input for adder.

The LFSR\_manager combine 3 output of LFSRs into 16-bits data.

* 1. MISR.v

The MISR compress the 17-bits result of adder into 10-bits signature.

My golden signature:

Signature 1 : 807

Signature 2 : 399

Signature 3 : 520

Signature 4 : 322

Signature 5 : 478

Signature 6 : 1010

Signature 7 : 283

Signature 8 : 680

Signature 9 : 883

Signature 10 : 731

Signature 11 : 657

Signature 12 : 361

Signature 13 : 977

Signature 14 : 1003

Signature 15 : 22

Signature 16 : 10

Signature 17 : 801

Signature 18 : 977

Signature 19 : 9

Signature 20 : 321

Signature 21 : 994

Signature 22 : 783

Signature 23 : 169

Signature 24 : 600

Signature 25 : 361

Signature 26 : 721

Signature 27 : 648

Signature 28 : 358

Signature 29 : 946

Signature 30 : 502

Signature 31 : 284

Signature 32 : 174

Signature 33 : 152

Signature 34 : 365

Signature 35 : 433

Signature 36 : 731

Signature 37 : 911

Signature 38 : 966

Signature 39 : 514

Signature 40 : 798

Signature 41 : 654

Signature 42 : 843

Signature 43 : 421

Signature 44 : 755

Signature 45 : 412

Signature 46 : 267

Signature 47 : 676

Signature 48 : 626

Signature 49 : 597

Signature 50 : 70

Signature 51 : 868

Signature 52 : 718

Signature 53 : 132

Signature 54 : 384

Signature 55 : 226

Signature 56 : 946

Signature 57 : 506

Signature 58 : 28

Signature 59 : 9

Signature 60 : 802

Signature 61 : 940

Signature 62 : 536

Signature 63 : 12

Signature 64 : 295

Signature 65 : 725

Signature 66 : 939

Signature 67 : 245

Signature 68 : 893

Signature 69 : 763

Signature 70 : 443

Signature 71 : 509

Signature 72 : 540

Signature 73 : 49

Signature 74 : 532

Signature 75 : 521

Signature 76 : 838

Signature 77 : 929

Signature 78 : 751

Signature 79 : 948

Signature 80 : 252

Signature 81 : 416

Signature 82 : 749

Signature 83 : 405

Signature 84 : 746

Signature 85 : 116

Signature 86 : 887

Signature 87 : 991

Signature 88 : 302

Signature 89 : 945

Signature 90 : 732

Signature 91 : 146

Signature 92 : 108

Signature 93 : 854

Signature 94 : 232

Signature 95 : 111

Signature 96 : 855

Signature 97 : 464

Signature 98 : 488

Signature 99 : 535

Signature 100 : 841

Signature 101 : 675

Signature 102 : 78

Signature 103 : 67

Signature 104 : 545

Signature 105 : 17

Signature 106 : 547

Signature 107 : 814

Signature 108 : 693

Signature 109 : 888

Signature 110 : 506

Signature 111 : 831

Signature 112 : 222

Signature 113 : 907

Signature 114 : 194

Signature 115 : 127

Signature 116 : 575

Signature 117 : 349

Signature 118 : 686

Signature 119 : 153

Signature 120 : 623

Signature 121 : 87

Signature 122 : 876

Signature 123 : 759

Signature 124 : 638

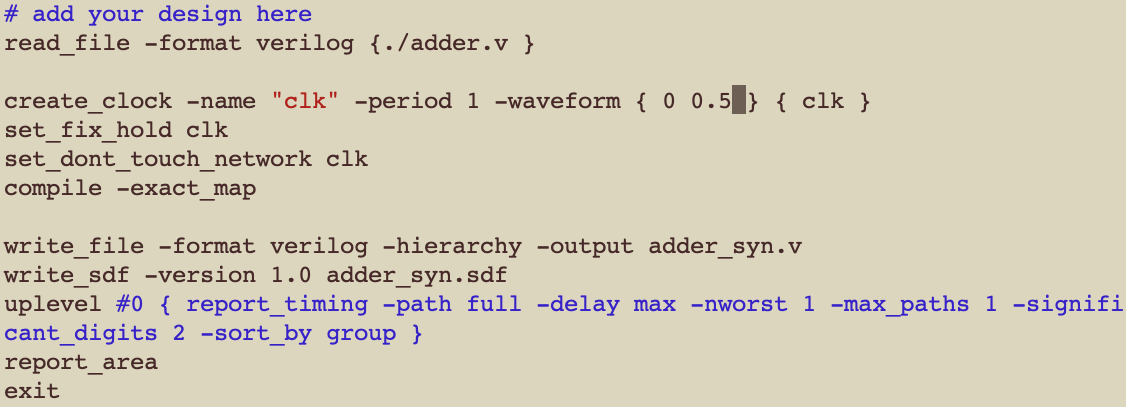
Signature 125 : 570

Signature 126 : 861

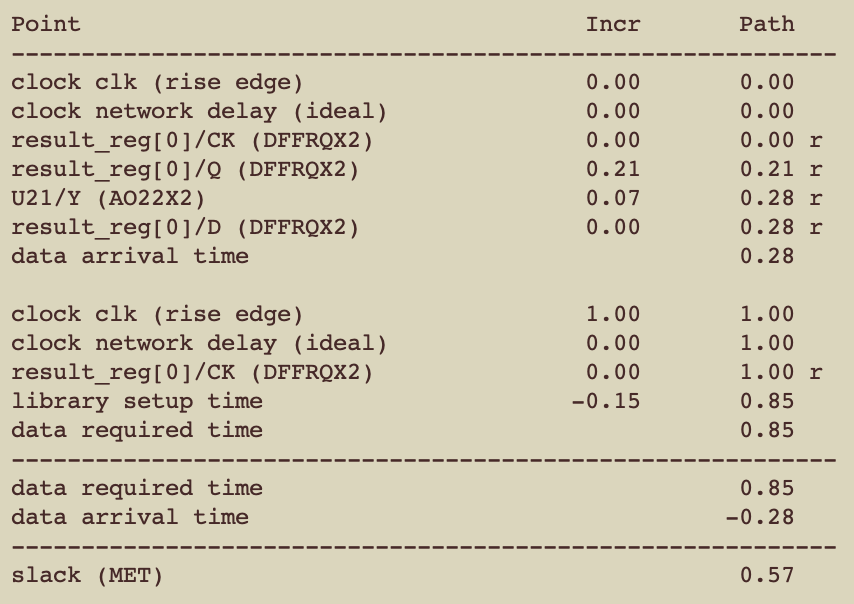
Signature 127 : 972

3. Test my adder whether it can operate at speed of 1 GHz.

Synthesis my adder with period = 1ns



<adder.dc>



< Timing report >

Simulation result:

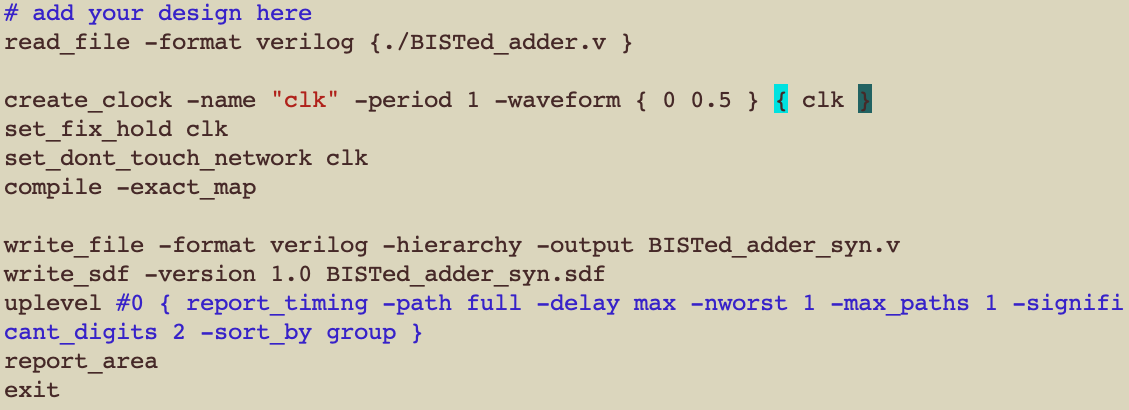
The adder is a netlist. Rest of modules are RTLs.

|  |  |  |  |
| --- | --- | --- | --- |
| Testbench timescale | 100ns/1ps | 10ns/1ps | 1ns/1ps |
| Result | pass | pass | pass |
|  |  |  |  |

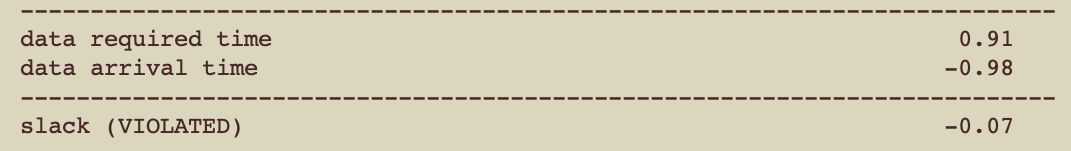
4. The maximum operating speed of my BISTed adder design

我把所有的module放進同一個file(BISTed\_adder.v)進行synthesis，從1 GHz開始測試synthesis的結果。

Synthesis with period = 1ns => fail

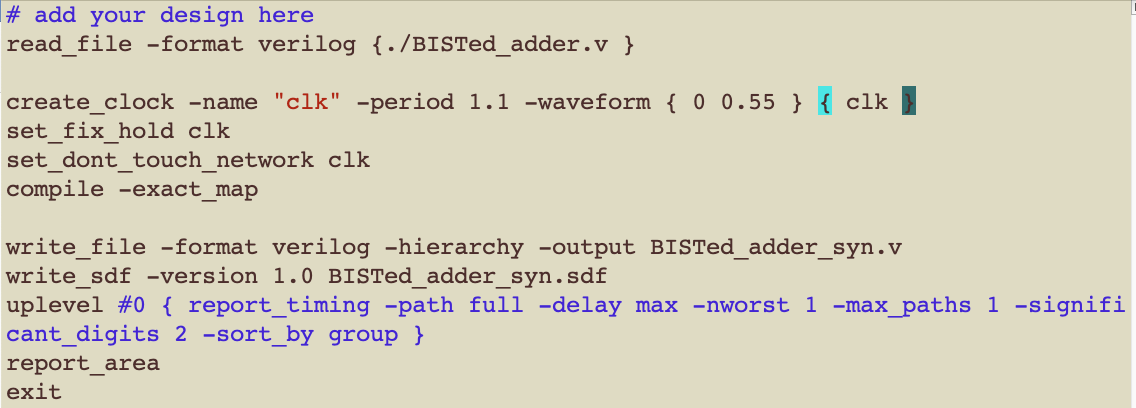


< BISTed\_adder.dc>

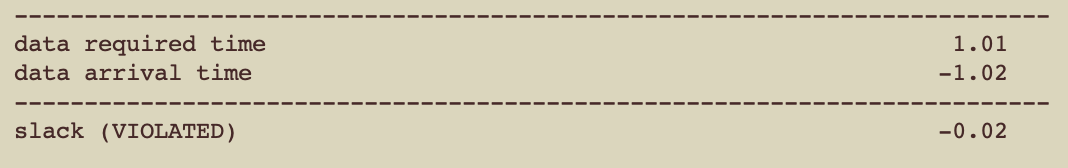


< Timing report >

Synthesis with period = 1.1ns => fail

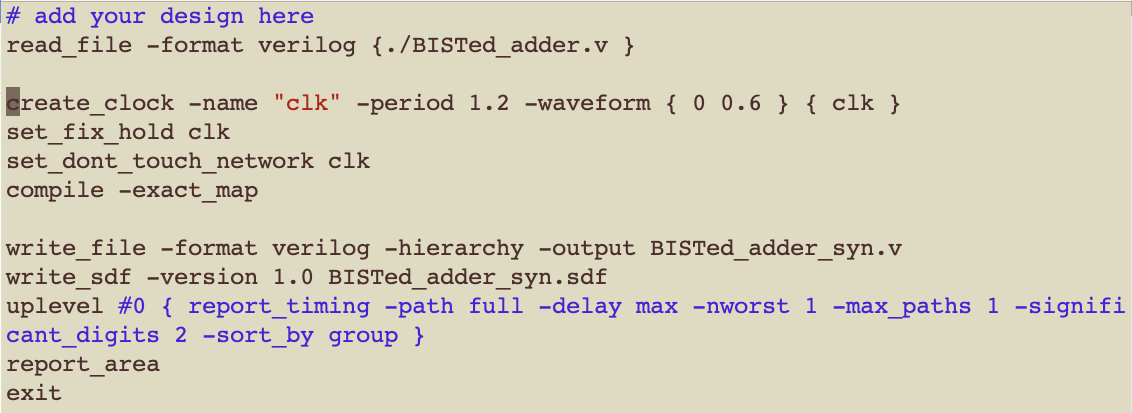


< BISTed\_adder.dc>

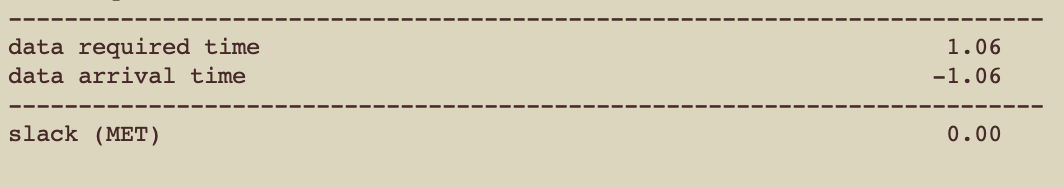


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Synthesis with period = 1.2ns => success

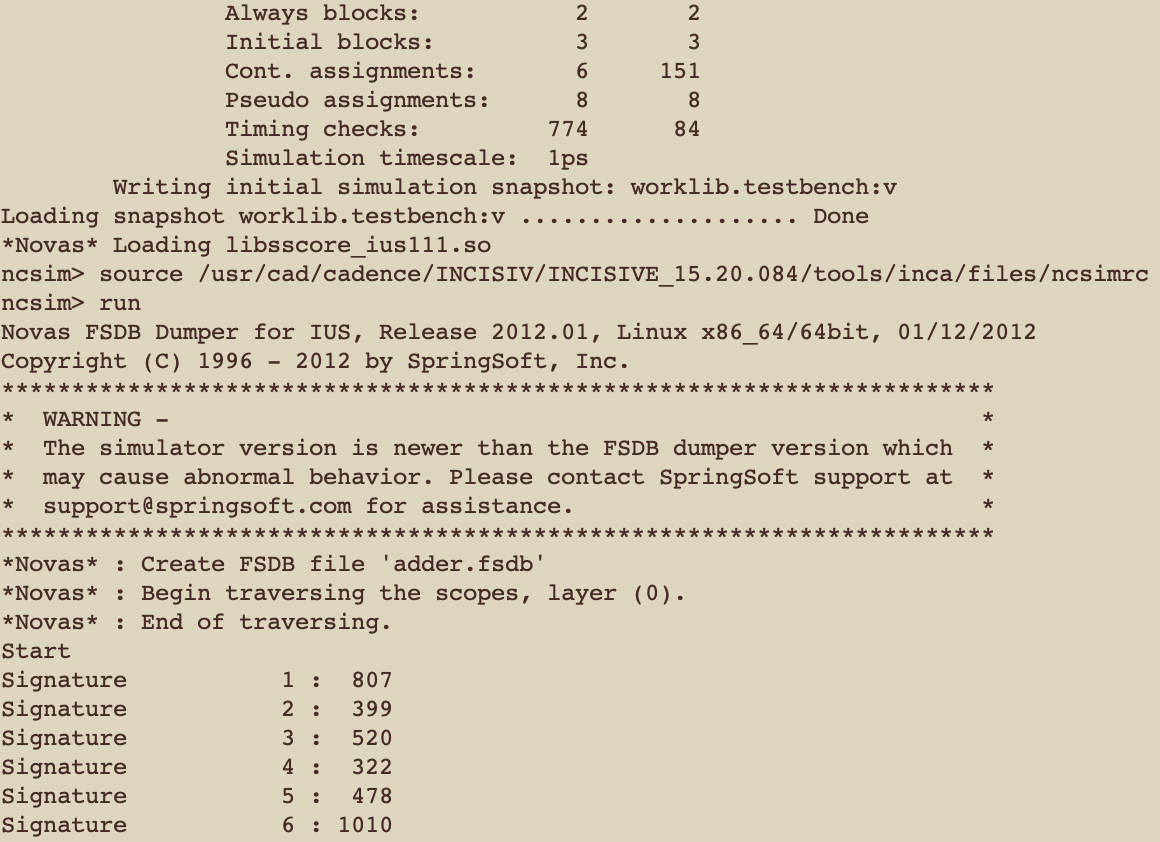


<BISTed\_adder.dc>



< Timing report >

Simulate the netlist which period = 1.2ns is successful.



The shortest period is 1.2ns => The max speed of my design is 0.83 GHz.